Access DB# 123660

SEARCH REQUEST FORM

Scientific and Technical Information Center

(14)

Requester's Full Name: _Jack Lane_____ Examiner # :_68699____ Date: 06/02/04____
Art Unit: _2188__ Phone Number 305-3818____ Serial Number: 09/394,222____
Mail Box Location: _2Y13_____ Results Format Preferred (circle): PAPER DISK E-MAIL

If more than one search is submitted, please prioritize searches in order of need.

****

Please provide a detailed statement of the search topic, and describe as specifically as possible the subject matter to be searched. Include the elected species or structures, keywords, synonyms, acronyms, and registry numbers, and combine with the concept or utility of the invention. Define any terms that may have a special meaning. Give examples or relevant citations, authors, etc, if known. Please attach a copy of the cover sheet, pertinent claims, and abstract.

Title of Invention: __System and Method for Re-Ordering Memory references in a Memory Control System to Speed Access To Memory Cells.

Inventors (please provide full names): William J. Dally, Scott W. Rixner,

Earliest Priority Filing Date: _09/14/98_____

***For Sequence Searches Only* Please include all pertinent information (parent, child, divisional, or issued patent numbers) along with the appropriate serial number.**

See the Abstract, claims and figure 4.

Essentially the invention is an address buffer that outputs addresses in an order different than the order in which they were received.

Search:

Buffer () address () order

****

STAFF USE ONLY

Searcher: David Holloway
Searcher Phone #: 308-7794
Searcher Location: CPK2 4B30

Type of Search

NA Sequence (#)_____
AA Sequence (#)_____
Structure (#) _____

Vendors and cost where applicable

STN _____
Dialog ✓
Questel/Orbit _____

```
Set     Items   Description
S1     318948   BUFFER? OR CACHE? OR TEMPORAR?()(STORAGE? OR MEMOR?)
S2    1398165   ADDRESS? OR LOCATION?
S3    6024882   CHANG? OR REARRANG? OR SORT OR RESORT OR REORDER? OR MODIF?
S4      13727   (NEW OR DIFFERENT)()(ORDER? OR ARRANGE?)
S5    6941643   ARRAY? OR CELL? OR STORAGE? OR MEMOR? OR RAM OR PROM OR EP-
            ROM OR EEPROM OR ROM
S6      36703   LIFO OR FIFO OR (LAST OR FIRST)()("IN" OR OUT)
S7          9   S1 (10N) S2 (4N) S3(2N)(ORDER? OR SEQUENC?)
S8          1   S1 AND S2 AND S4
S9       2331   S2 AND (S3 OR S4) AND S1
S10        34   S2(2N)S3 AND S6
S11      1290   S9 AND S5
S12        75   S2(2N)S3 AND S11
S13       116   S7 OR S8 OR S10 OR S12
S14        87   RD (unique items)
S15        50   S14 NOT PY>1998
File   8:Ei Compendex(R) 1970-2004/May W5
         (c) 2004 Elsevier Eng.  Info. Inc.
File  35:Dissertation Abs Online 1861-2004/May
         (c) 2004 ProQuest Info&Learning
File  65:Inside Conferences 1993-2004/Jun W1
         (c) 2004 BLDSC all rts. reserv.
File   2:INSPEC 1969-2004/May W5
         (c) 2004 Institution of Electrical Engineers
File  94:JICST-EPlus 1985-2004/May W2
         (c)2004 Japan Science and Tech Corp(JST)
File 111:TGG Natl.Newspaper Index(SM) 1979-2004/Jun 07
         (c) 2004 The Gale Group
File 233:Internet & Personal Comp. Abs. 1981-2003/Sep
         (c) 2003 EBSCO Pub.
File   6:NTIS 1964-2004/Jun W1
         (c) 2004 NTIS, Intl Cpyrght All Rights Res
File 144:Pascal 1973-2004/May W5
         (c) 2004 INIST/CNRS
File  34:SciSearch(R) Cited Ref Sci 1990-2004/May W5
         (c) 2004 Inst for Sci Info
File  99:Wilson Appl. Sci & Tech Abs 1983-2004/Apr
         (c) 2004 The HW Wilson Co.
File  95:TEME-Technology & Management 1989-2004/May W4
         (c) 2004 FIZ TECHNIK
```

15/5/9 (Item 9 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

00950548 E.I. Monthly No: EI8009065267 E.I. Yearly No: EI80007813

Title: ONE YEAR EXPERIENCE WITH A HIGH RESOLUTION RING DETECTOR POSITRON CAMERA SYSTEM: PRESENT STATUS AND FUTURE PLANS.

Author: Eriksson, L.; Bohm, Chr.; Bergstrom, M.; Ericson, K.; Greitz, T.; Litton, J.; Widen, L.

Corporate Source: Univ of Stockholm, Swed

Source: IEEE Transactions on Nuclear Science v NS-27 n 1 Feb 1980, Nucl Sci Symp, 26th, and Symp on Nucl Power Syst, 11th, San Francisco, Calif, Oct 17-19 1979 p 435-444

Publication Year: 1980

CODEN: IETNAE ISSN: 0018-9499

Language: ENGLISH

Journal Announcement: 8009

Abstract: A ring detctor positron camera system for brain research is described. The system utilizes 95 8 X 20 X 50 mm NaI (T1) detectors and is simultaneously recording coincidences from 1900 detection channels over a 30 cm diameter image field. To improve sampling two motions of the detector ring are utilized: a small rotation of half a crystal distance combined with a wobbling motion. The time window of the detection channels for accepting coincidences is 22 ns. Each detection channel corresponds to a unique **address** which labels any recorded event. Before being temporarily stored in a **buffer memory** the event **address** passes through a **PROM** module which (1) removes events outside the specified image field and, (2) **rearranges** the event **address** to a projection **address** , i. e. a hardware preprocessing of incoming data. The effective intrinsic resolution is 5. 5 mm at the center of the image field and, together with a four point wobble, an overall resolution of 7 mm is obtained. 7 refs.

Descriptors: *BIOMEDICAL ENGINEERING--*Imaging Techniques; BIOMEDICAL EQUIPMENT

Classification Codes:

461 (Biotechnology)

15/5/30 (Item 12 from file: 2)
DIALOG(R)File 2:INSPEC

00170427 INSPEC Abstract Number: C70017621
Title: Computer instruction address modifier
Assignee(s): General Electric Co
Patent Number: GB 1179048 Issue Date: 700128
Application Date: 670609
Priority Appl. Number: US 560572 Priority Appl. Date: 660627
Country of Publication: UK
Language: English Document Type: Patent (PT)
Abstract: An indirect instruction **address** is **modified** each time it is fetched from memory. A tally portion of the indirect instruction is also modified, and the modified indirect instruction is stored at the location specified by the address portion of the first instruction before the memory is accessed by the address portion of the indirect instruction to initiate the operation specified by the first instruction. The tally portion of the indirect instruction is hanged by the same **modifier** as the **address** portion, the **modified** tally portion is stored in an address register while the address portion is being modified, and the **modified address** and tally portions are simultaneously transferred to memory. At least two of the possible modifications are complementary for addressing the same indirect instruction and include modifications in which the indirect instruction address is incremented or decremented to provide **last - in - first - out** memory accessing.
Subfile: C
Descriptors: data acquisition
Class Codes: C6130 (Data handling techniques)

15/5/32 (Item 1 from file: 233)
DIALOG(R)File 233:Internet & Personal Comp. Abs.

00390847 95BY07-022

HP's speedy RISC -- Numerous function units and smart load/store processing make the PA-8000 the fastest RISC processor

Pountain, Dick

BYTE , July 1, 1995 , v20 n7 p175-176, 2 Page(s)
ISSN: 0360-5280

Company Name: Hewlett-Packard
Product Name: PA-8000
Languages: English
Document Type: Feature Articles and News
Geographic Location: United States

Describes the new PA-8000 RISC processor from Hewlett-Packard, which may be the fastest RISC architecture in the world. Explains that the PA-8000's design aims for ``sustainable superscalar'' operation by employing multiple function units and a radical out-of-order execution strategy that executes four instructions simultaneously most of the time. Indicates that the PA-8000's microarchitecture is entirely new; it contains an extremely fast, 960 Mbps 64-bit Runway processor bus; and it keeps the instruction and data **caches** off-chip. Notes that this chip's out-of-order execution is achieved by its use of hardware scheduling to extract the maximum parallelism from the instruction stream; and that its instruction-fetch unit fetches blocks of four quadword-aligned instructions per cycle from the external I- **cache** . Discusses the PA-8000's 56 rename registers and **storage** of **addresses** into the 28-slot **address reorder buffer** . Includes two diagrams. (jo)

Descriptors: RISC Technology; Microprocessor; Caching; Architecture; 64-Bit; Parallel Processing
Identifiers: PA-8000; Hewlett-Packard

```
Set      Items   Description
S1        1118   BUFFER? OR CACHE? OR TEMPORAR?()(STORAGE? OR MEMOR?)
S2       11263   ADDRESS? OR LOCATION?
S3       14233   CHANG? OR REARRANG? OR SORT OR RESORT OR REORDER? OR MODIF?
S4          36   (NEW OR DIFFERENT)()(ORDER? OR ARRANGE?)
S5       14224   ARRAY? OR CELL? OR STORAGE? OR MEMOR? OR RAM OR PROM OR EP-
             ROM OR EEPROM OR ROM
S6         162   LIFO OR FIFO OR (LAST OR FIRST)()("IN" OR OUT)
S7           0   S1 (10N) S2 (4N) S3(2N)(ORDER? OR SEQUENC?)
S8           0   S1 (4N)S2 (4N) S4
S9           0   S1(5N)S2(5N)S4
S10          0   S1(10N)S2(10N)S4(10N)S5(10N)S6
S11        208   S3(2N)(ORDER? OR SEQUENC? OR ARRANGEMENT? OR RECEIVED) OR -
              S4
S12          2   S1 AND (S2(3N)S3 OR S4)
S13          1   S11 AND (S1 OR S6)
S14          3   S12 OR S13
File 256:SoftBase:Reviews,Companies&Prods. 82-2004/May
         (c)2004 Info.Sources Inc
```

Set	Items	Description
S1	266361	BUFFER? OR CACHE? OR TEMPORAR?()(STORAGE? OR MEMOR?)
S2	548878	ADDRESS? OR LOCATION?
S3	1601597	CHANG? OR REARRANG? OR SORT OR RESORT OR REORDER? OR MODIF?
S4	12168	(NEW OR DIFFERENT)()(ORDER? OR ARRANGE?)
S5	961850	ARRAY? OR CELL? OR STORAGE? OR MEMOR? OR RAM OR PROM OR EPROM OR EEPROM OR ROM
S6	59063	LIFO OR FIFO OR (LAST OR FIRST)()("IN" OR OUT)
S7	391	S1 (10N) S2 (4N) S3(2N)(ORDER? OR SEQUENC?)
S8	0	S1 (4N)S2 (4N) S4
S9	1	S1(5N)S2(5N)S4
S10	1	S1(10N)S2(10N)S4(10N)S5(10N)S6
S11	83099	S3(2N)(ORDER? OR SEQUENC? OR ARRANGEMENT? OR RECEIVED) OR S4
S12	180	S11(10N)S6
S13	35	S12(S)S1
S14	67	S12(S)S5
S15	37	S7(S)S6
S16	21	S7(10N)S6
S17	113	S9 OR S10 OR S13 OR S14 OR S15 OR S16
S18	12	S17 AND IC=(G06F-012/00 OR G06F-012/14 OR G06F-012/16 OR G06F-013/00 OR G06F-013/28)
S19	23	S17 AND IC=(G06F-012? OR G06F-013?)
S20	16	S19 NOT AD=19980914:20010914
S21	16	S20 NOT AD=20010914:20040609
S22	16	IDPAT (sorted in duplicate/non-duplicate order)
S23	16	IDPAT (primary/non-duplicate records only)

File 348:EUROPEAN PATENTS 1978-2004/Jun W01
(c) 2004 European Patent Office
File 349:PCT FULLTEXT 1979-2002/UB=20040603,UT=20040527
(c) 2004 WIPO/Univentio

23/3,K/2 **(Item 2 from file: 348)**
DIALOG(R)File 348:EUROPEAN PATENTS

00877646
Method of configuring a data packet transfer device
Verfahren zur Konfiguration eines Datenpaketubertragungsgerates
Procede pour configurer un dispositif de transfert de paquets de donnees
PATENT ASSIGNEE:
TEXAS INSTRUMENTS INCORPORATED, (279075), 13510 North Central Expressway, Dallas, Texas 75243, (US), (applicant designated states: DE;FR;GB;IT;NL)
INVENTOR:
Baker, Richard T., 3003 Silverleaf Drive, Austin, Texas 78757, (US)
LEGAL REPRESENTATIVE:
Holt, Michael (50421), Texas Instruments Limited, P.O. Box 5069, Northampton NN4 7ZE, (GB)
PATENT (CC, No, Kind, Date): EP 803803 A2 971029 (Basic)
EP 803803 A3 990428
APPLICATION (CC, No, Date): EP 97302797 970424;
PRIORITY (CC, No, Date): US 16518 960430
DESIGNATED STATES: DE; FR; GB; IT; NL
INTERNATIONAL PATENT CLASS: G06F-009/445; **G06F-013/12** ; **G06F-013/28**
ABSTRACT WORD COUNT: 87
LANGUAGE (Publication,Procedural,Application): English; English; English
FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS A	(English)	9710W4	688
SPEC A	(English)	9710W4	17099
Total word count - document A			17787
Total word count - document B			0
Total word count - documents A + B			17787

...INTERNATIONAL PATENT CLASS: **G06F-013/12** ...

... **G06F-013/28**

...SPECIFICATION the quadlet data read from the FIFO into individually selectable bytes for writing to host **memory** on byte-aligned addresses by the active DMA channel. This logic consists of four 8...

...to an output byte lane which is switched by the DMA channel to the host **memory** . For each of the 8-to-1 multiplexers, four inputs connect in a one-to...to-one correspondence to each register input. This configuration allows the quadlet read from the **FIFO** to be cross-point switched in a **different order** onto the output byte lanes. The control of the byte lane multiplexers is by the...

23/3,K/6 **(Item 6 from file: 348)**
DIALOG(R)File 348:EUROPEAN PATENTS

00711606
Start code detector for image sequences
Detektor fur den Startcode von Bildsequenzen
Detecteur de code de depart pour sequences d'images
PATENT ASSIGNEE:
DISCOVISION ASSOCIATES, (260273), 2355 Main Street Suite 200, Irvine, CA 92714, (US), (Proprietor designated states: all)
INVENTOR:
Wise, Adrian Philip, 10 Westbourne Cottages, Frenchay, Bristol BS16 1NA, (GB)
Sotheran, Martin William, The Ridings, Wick Lane, Stinchcombe, Dursley, Gloucestershire GL11 6BD, (GB)
Robbins, William Philip, 19 Springhill, Cam, Gloucestershire GL11 5PE, (GB)
Finch, Helen Rosemary, Tyley, Coombe, Wotton-Under-Edge, Gloucester. GL12 7ND, (GB)
Boyd, Kevin James, 21 Lancashire Road, Bristol BS7 9DL, (GB)
LEGAL REPRESENTATIVE:
Vuillermoz, Bruno et al (72791), Cabinet Laurent & Charras B.P. 32 20, rue Louis Chirpaz, 69131 Ecully Cedex, (FR)
PATENT (CC, No, Kind, Date): EP 674443 A2 950927 (Basic)
EP 674443 A3 951213
EP 674443 A3 981223
EP 674443 B1 010509
APPLICATION (CC, No, Date): EP 95301301 950228;
PRIORITY (CC, No, Date): GB 9405914 940324
DESIGNATED STATES: AT; BE; CH; DE; FR; GB; IE; IT; LI; NL
RELATED DIVISIONAL NUMBER(S) - PN (AN):
EP 891089 (EP 98202149)
(EP 98202154)
EP 884910 (EP 98202132)
EP 891088 (EP 98202133)
EP 897244 (EP 98202134)
EP 901286 (EP 98202135)
EP 901287 (EP 98202166)
EP 896473 (EP 98202170)
EP 896474 (EP 98202171)
EP 896476 (EP 98202174)
EP 896475 (EP 98202172)
INTERNATIONAL PATENT CLASS: H04N-007/24; **G06F-013/00** ; G06F-009/38
ABSTRACT WORD COUNT: 102
NOTE:
Figure number on first page: 61

LANGUAGE (Publication,Procedural,Application): English; English; English
FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS A	(English)	EPAB95	2897
CLAIMS B	(English)	200119	647
CLAIMS B	(German)	200119	609
CLAIMS B	(French)	200119	752
SPEC A	(English)	EPAB95	128616
SPEC B	(English)	200119	122384
Total word count - document A			131543
Total word count - document B			124392
Total word count - documents A + B			255935

...INTERNATIONAL PATENT CLASS: **G06F-013/00**

...SPECIFICATION starts to be decoded by the Temporal Decoder.
As the P or I pictures are **reordered** , certain tokens are stored temporarily on chip as the picture is written into the picture **buffers** . When the picture is read out for display, these stored tokens are retrieved. At the...addresses as the result of receiving control tokens,

or it may merely generate a fixed **sequence** of **addresses** (e.g., for the **FIFO buffers** of the Spatial Decoder). The DRAM interface treats the two wire interfaces associated with the **address** generator 301 in a special way. Instead of keeping the accept line high when it...

23/3,K/8 **(Item 8 from file: 348)**
DIALOG(R)File 348:EUROPEAN PATENTS

00602538

Programmable external storage control apparatus
Programmierbare Externspeichersteuerungseinrichtung
Dispositif de commande programmable pour memoire externe

PATENT ASSIGNEE:
International Business Machines Corporation, (200120), Old Orchard Road, Armonk, N.Y. 10504, (US), (applicant designated states: DE;FR;GB)
INVENTOR:
Numata, Tsutomu, 1108-13, Isobe, Sagamihara-shi, Kanagawa-ken, (JP)
Kigami, Yuji, Arusuyamato 204, 2-5-12 Shimotsuruma, Yamato-shi, Kanagawa-ken 242, (JP)
Sakai, Tatsuya, 7-28-1-103, Higashi-rinkan, Sagamihara-shi, Kanagawa-ken, (JP)
Shimizu, Kenji, 2-21-15, Chuou-rinkan, Yamato-shi, Kanagawa-ken, (JP)
LEGAL REPRESENTATIVE:
Moss, Robert Douglas (34141), IBM United Kingdom Limited Intellectual Property Department Hursley Park, Winchester Hampshire SO21 2JN, (GB)
PATENT (CC, No, Kind, Date): EP 598541 A1 940525 (Basic)
EP 598541 B1 990728
APPLICATION (CC, No, Date): EP 93308943 931109;
PRIORITY (CC, No, Date): JP 30835392 921118
DESIGNATED STATES: DE; FR; GB
INTERNATIONAL PATENT CLASS: G06F-009/44; G06F-003/06; **G06F-013/12**
ABSTRACT WORD COUNT: 125

LANGUAGE (Publication,Procedural,Application): English; English; English
FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS B	(English)	9930	889
CLAIMS B	(German)	9930	838
CLAIMS B	(French)	9930	1085
SPEC B	(English)	9930	7065
Total word count - document A			0
Total word count - document B			9877
Total word count - documents A + B			9877

...INTERNATIONAL PATENT CLASS: **G06F-013/12**

...SPECIFICATION WP 76 satisfy the above condition.
When five words have been transferred from the disk **FIFO** 56 to the sector buffer 16, the memory timing control circuit 68 starts transfer from the sector buffer 16 to the **sequencer FIFO** 58 by **changing** the access of the sector **buffer** 16 to the **sequencer** phase and enabling the **sequencer address** counter 66. The **sequencer address** counter 66 is preset to a start address of the program storage area 16B, that...

...control program and the first to sixth instruction words are continuously transferred to the sequencer **FIFO** 58 in the sequencer phase. The memory timing control circuit 68 performs such transfer by...

...value (e.g. 3), the memory timing control circuit 68 starts transfer from the sequencer **FIFO** 58 to the sequencer 28. The sequencer 28 reads the sequencer **FIFO** 58 by incrementing the RP 78 one by one. When six words have been transferred from the sector buffer 16 to the sequencer **FIFO** , the memory timing control circuit 68 changes again to the disk phase.
When a sector...

23/3,K/16 **(Item 16 from file: 349)**
DIALOG(R)File 349:PCT FULLTEXT

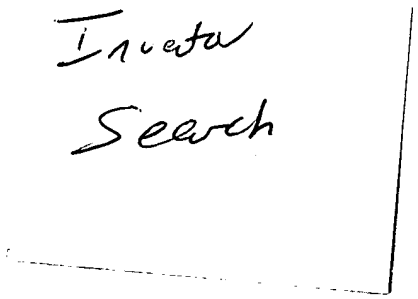
00207472 **Image available**
IMPROVED MEMORY SYSTEM
SYSTEME DE MEMOIRE AMELIORE
Patent Applicant/Assignee:
HYATT Gilbert P,
Inventor(s):
HYATT Gilbert P,
Patent and Priority Information (Country, Number, Date):
Patent: WO 9204673 A1 19920319
Application: WO 91US6285 19910903 (PCT/WO US9106285)
Priority Application: US 9041 19900904
Designated States: AT BE CA CH DE DK ES FR GB GR IT JP KR LU NL SE
Publication Language: English
Fulltext Word Count: 137004

Main International Patent Class: **G06F-012/02**
Fulltext Availability:
Detailed Description

Detailed Description
... shorter scanout propagation delays and a single longer address propagation delay.

Speed is enhanced by **changing** the clock period to be a function of the **addressing** operation, such as a longer clock period for re- **addressing** and a shorter clock period for scanout. A **buffer** memory, such as a **FIFO** , double **buffer** , **cache** , or scratchpad memory; can be used to **buffer** output information
from the memory for providing a constant memory output clock period in response...

```
Set     Items   Description
S1         62   AU=(DALLY W? OR DALLY, W?)
S2          7   S1 AND IC=(G06F-012? OR G06F-013?)
S3          7   IDPAT (sorted in duplicate/non-duplicate order)
S4          7   IDPAT (primary/non-duplicate records only)
File 347:JAPIO Nov 1976-2004/Jan(Updated 040506)
         (c) 2004 JPO & JAPIO
File 348:EUROPEAN PATENTS 1978-2004/Jun W01
         (c) 2004 European Patent Office
File 349:PCT FULLTEXT 1979-2002/UB=20040603,UT=20040527
         (c) 2004 WIPO/Univentio
File 350:Derwent WPIX 1963-2004/UD,UM &UP=200435
         (c) 2004  Thomson Derwent
```



4/5/2 (Item 2 from file: 350)

012933158 **Image available**
WPI Acc No: 2000-105005/200009
Related WPI Acc No: 1999-045120
XRPX Acc No: N00-080657

Virtual addressing method in parallel data processing system

Patent Assignee: MASSACHUSETTS INST TECHNOLOGY (MASI)
Inventor: CARTER N P; **DALLY W J** ; KECKLER S W
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
US 6003123	A	19991214	US 94314013	A	19940928	200009 B
			US 9821658	A	19980210	

Priority Applications (No Type Date): US 94314013 A 19940928; US 9821658 A 19980210
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6003123	A		28	G06F-012/10	Div ex application US 94314013 Div ex patent US 5845331

Abstract (Basic): US 6003123 A

NOVELTY - A virtual address (VA) is applied to a global translational buffer, to identify page group mapping to nodes in a system. From the virtual address and mapping, the destination node is determined and the virtual address is converted into physical address. The buffer identifies the page groups by the group size encoded logarithmically. The start node and number of pages per group is specified by the buffer.

DETAILED DESCRIPTION - An INDEPENDENT CLAIM is included for a data processing system.

USE - For virtual addressing and sharing of data across multiple nodes of parallel data processing system.

ADVANTAGE - Provides guarded pointers which perform efficient protection and sharing of data. Because memory is accessed directly using guarded pointers, higher performance is achieved than with traditional implementations of capabilities, as table look ups to translate capabilities to virtual addresses, are not required.

DESCRIPTION OF DRAWING(S) - The figure shows the GTLB entry in a global translation buffer.

pp; 28 DwgNo 13/17

Title Terms: VIRTUAL; ADDRESS; METHOD; PARALLEL; DATA; PROCESS; SYSTEM
Derwent Class: T01
International Patent Class (Main): **G06F-012/10**
File Segment: EPI

012239012 **Image available**
WPI Acc No: 1999-045120/199904
Related WPI Acc No: 2000-105005
XRPX Acc No: N99-033018

Data processing system - uses guarded pointers for addressing memory locations with restricted access, distinguishes from other words by processor network and modifies, preventing access beyond protected segment of memory

Patent Assignee: MASSACHUSETTS INST TECHNOLOGY (MASI)
Inventor: CARTER N P; **DALLY W J** ; KECKLER S W
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 5845331	A	19981201	US 94314013	A	19940928	199904	B

Priority Applications (No Type Date): US 94314013 A 19940928
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 5845331	A		29	G06F-012/10	

Abstract (Basic): US 5845331 A

The system includes a shared memory for storing instruction and data for multiple programs, which is accessed in response to pointers. Several guarded pointers are provided for addressing memory locations with restricted access. Each guarded pointer comprises a processor word for complete identification of a protected segment of memory and a virtual address within the protected segment, without table look-up.

A processor network is used for distinguishing guarded pointers from other words, which is operable under program control to modify the guarded pointers. The modification of the guarded pointers is restricted to prevent access beyond the protected segment.

USE - In virtual addressing, multiprocessor environment.

ADVANTAGE - Enables global addressing across multiple processor nodes. Provides security for allowing common access to certain memory locations, while protecting against unauthorised access to other locations. Eliminates need for changing translation scheme on context switches and facilitates use of virtually addressed caches.

Dwg.1A/17

Title Terms: DATA; PROCESS; SYSTEM; GUARD; POINT; ADDRESS; MEMORY; LOCATE; RESTRICT; ACCESS; DISTINGUISH; WORD; PROCESSOR; NETWORK; MODIFIED; PREVENT; ACCESS; PROTECT; SEGMENT; MEMORY
Derwent Class: T01
International Patent Class (Main): **G06F-012/10**
File Segment: EPI

4/5/6 (Item 6 from file: 350)
DIALOG(R)File 350:Derwent WPIX

009482215 **Image available**
WPI Acc No: 1993-175750/199321
XRPX Acc No: N93-134748

Message driven processor in concurrent computer - including storing input in raw buffer and translator cache located in main memory with its output directed through set of comparators

Patent Assignee: MASSACHUSETTS INST TECHNOLOGY (MASI)
Inventor: CHIEN A A; **DALLY W J** ; FISKE S; HORWAT W P
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 5212778	A	19930518	US 88200003	A	19880527	199321	B

Priority Applications (No Type Date): US 88200003 A 19880527
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 5212778	A		14	G06F-015/16	

Abstract (Basic): US 5212778 A

The concurrent computer system, the method in a processor of the array comprises: automatically storing sequential messages in a queue independent of any ongoing routine; with suspension of a routine, reading a header of a next received message from the queue, and from a physical address in the header directly addressing a first handler routine to be processed.

The first handler routine and subsequent routines to which the first handler routine directs the processor are processed the first handler routine processing data in the message to locate a subsequent routine. A segment of a memory is identified by creating a segment descriptor that identifies a base address and a length of the entire week received message from length data in the header. Message arguments under program control area read from the identified memory segment by computing an address as an offset from the base address from the segment descriptor and checking the address against a length limit.

USE/ADVANTAGE - Message-driven MIMD systems. Minimised memory access and increased throughput.

6,7,8/12

Title Terms: MESSAGE; DRIVE; PROCESSOR; CONCURRENT; COMPUTER; STORAGE; INPUT; RAW; BUFFER; TRANSLATION; CACHE; LOCATE; MAIN; MEMORY; OUTPUT; DIRECT; THROUGH; SET; COMPARATOR
Derwent Class: T01
International Patent Class (Main): G06F-015/16
International Patent Class (Additional): G06F-009/32; **G06F-012/06** ; **G06F-013/00**
File Segment: EPI

```
Set     Items   Description
S1     205783   BUFFER? OR CACHE? OR TEMPORAR?()(STORAGE? OR MEMOR?)
S2    2977794   ADDRESS? OR LOCATION?
S3    4877693   CHANG? OR REARRANG? OR SORT OR RESORT OR REORDER? OR MODIF?
S4     168491   (NEW OR DIFFERENT)()(ORDER? OR ARRANGE?)
S5    3110587   ARRAY? OR CELL? OR STORAGE? OR MEMOR? OR RAM OR PROM OR EP-
            ROM OR EEPROM OR ROM
S6      14684   FIFO OR LIFO
S7       8703   FIRST()OUT
S8      20783   (S6 OR S7)
S9         20   S1(10N)S2(2N)S3(2N)(ORDER? OR SEQUENCE?)
S10         1   S1(10N)S2(10N)S4
S11        16   S8(S)(S2(2N)S3 OR S4)
S12         4   S1(S)S2(S)S4
S13        40   S9 OR S10 OR S11 OR S12
S14        31   RD (unique items)
S15        24   S14 NOT PY>1998
S16        23   S15 NOT PD=19980914:20010914
S17        23   S16 NOT PD=20010914:20040609
File 275:Gale Group Computer DB(TM) 1983-2004/Jun 08
         (c) 2004 The Gale Group
File  47:Gale Group Magazine DB(TM) 1959-2004/Jun 03
         (c) 2004 The Gale group
File 636:Gale Group Newsletter DB(TM) 1987-2004/Jun 07
         (c) 2004 The Gale Group
File  16:Gale Group PROMT(R) 1990-2004/Jun 08
         (c) 2004 The Gale Group
File 624:McGraw-Hill Publications 1985-2004/Jun 07
         (c) 2004 McGraw-Hill Co. Inc
File 613:PR Newswire 1999-2004/Jun 08
         (c) 2004 PR Newswire Association Inc
File 813:PR Newswire 1987-1999/Apr 30
         (c) 1999 PR Newswire Association Inc
File 696:DIALOG Telecom. Newsletters 1995-2004/Jun 07
         (c) 2004 The Dialog Corp.
File 621:Gale Group New Prod.Annou.(R) 1985-2004/Jun 04
         (c) 2004 The Gale Group
File 674:Computer News Fulltext 1989-2004/May W4
         (c) 2004 IDG Communications
```

17/3,K/7 **(Item 7 from file: 275)**
DIALOG(R)File 275:Gale Group Computer DB(TM)

01531029 SUPPLIER NUMBER: 12475842 (USE FORMAT 7 OR 9 FOR FULL TEXT)
High-performance designs for the low-cost PA-RISC desktop. (processor, memory, graphics, multimedia and built-in core I/O design of new HP 9000 Models 705 and 710 entry-level workstations) (Technical)
Frink, Craig R.; Hammond, Robert J.; Dykstal, John A.; Soltis, Don C. Jr.
Hewlett-Packard Journal, v43, n4, p55(9)
August, 1992
DOCUMENT TYPE: Technical ISSN: 0018-1153 LANGUAGE: ENGLISH
RECORD TYPE: FULLTEXT; ABSTRACT
WORD COUNT: 6091 LINE COUNT: 00492

... pixels down the 32-bit bus. Next, the system bus interface sends a beginning frame **buffer address** . Finally, a **sequence** of data packets follows, accompanied by an **address modification** rule. The frame **buffer** controller uses this **address modification** rule to synthesize the **addresses** of subsequent pixels.

The system bus interface provides a second important function--it contains hardware...

17/3,K/19 **(Item 5 from file: 16)**
DIALOG(R)File 16:Gale Group PROMT(R)

01905991 Supplier Number: 42426334 (USE FORMAT 7 FOR FULLTEXT)
VMEbus and Multibus II slug it out
Electronic World News, p28
Oct 7, 1991
Language: English Record Type: Fulltext
Document Type: Magazine/Journal; Trade
Word Count: 2861

... Group, believes that, "implemantation-wise, SSBLT is significantly simpler than MBLT. It's basically a **FIFO** sitting on the bus interface and some design rules for making the **FIFO** work at a certain rate." If it is determined (through a dialogue of **address - modifier** codes) that an SSBLT between two boards can take place, "the master drives the data...

17/3,K/21 **(Item 7 from file: 16)**
DIALOG(R)File 16:Gale Group PROMT(R)

01367758 Supplier Number: 41621897 (USE FORMAT 7 FOR FULLTEXT)
NCR INTRODUCES NEW GENERATION OF HIGH-PERFORMANCE VGA DISPLAY CONTROLLER CHIPS
News Release, p1
Oct 22, 1990
Language: English Record Type: Fulltext
Document Type: Magazine/Journal; Trade
Word Count: 828

... for ergonomic-sensitive markets. Wide
font support also permits improved text quality without application
software **changes** . The 77C22 can support up to 4 Mbytes of frame
buffer memory easily supporting extended display modes, multi-tasked
video and animated **sequences** . Special **addressing**
logic allows simple
flame **buffer** copying and automatic offset **addressing** . The 77C22
supports various memory configurations for easy frame **buffer** design.

High-performance 16-bit BIOS, with emphasis toward graphics modes,
includes text support for...

```
Set     Items   Description
S1        565   AU=(DALLY W? OR DALLY, W?)
S2        137   S1 AND (MEMOR? OR CACHE? OR BUFFER? OR TEMPORAR?()STORAGE?)
S3         26   S2 AND (ADDRESS? OR LOCATION?)
S4         15   RD (unique items)
File   2:INSPEC 1969-2004/May W5
         (c) 2004 Institution of Electrical Engineers
File   6:NTIS 1964-2004/Jun W1
         (c) 2004 NTIS, Intl Cpyrght All Rights Res
File   8:Ei Compendex(R) 1970-2004/May W5
         (c) 2004 Elsevier Eng.  Info. Inc.
File  34:SciSearch(R) Cited Ref Sci 1990-2004/May W5
         (c) 2004 Inst for Sci Info
File  35:Dissertation Abs Online 1861-2004/May
         (c) 2004 ProQuest Info&Learning
File  65:Inside Conferences 1993-2004/Jun W1
         (c) 2004 BLDSC all rts. reserv.
File 636:Gale Group Newsletter DB(TM) 1987-2004/Jun 04
         (c) 2004 The Gale Group
File 275:Gale Group Computer DB(TM) 1983-2004/Jun 07
         (c) 2004 The Gale Group
File  94:JICST-EPlus 1985-2004/May W2
         (c)2004 Japan Science and Tech Corp(JST)
File 148:Gale Group Trade & Industry DB 1976-2004/Jun 07
         (c)2004 The Gale Group
File 674:Computer News Fulltext 1989-2004/May W4
         (c) 2004 IDG Communications
File 647:CMP  Computer Fulltext 1988-2004/May W4
         (c) 2004 CMP Media, LLC
```

4/5,K/1 (Item 1 from file: 2)
DIALOG(R)File 2:INSPEC

6977540 INSPEC Abstract Number: C2001-08-5220P-039
Title: Processor mechanisms for software shared memory
Author(s): Carter, N.P.; **Dally, W.J.** ; Lee, W.S.; Keckler, S.W.; Chang, A.
Author Affiliation: Coordinated Sci. Lab., Illinois Univ., Urbana, IL, USA
Conference Title: High Performance Computing. Third International Symposium, ISHPC 2000. Proceedings (Lecture Notes in Computer Science Vol.1940) p.120-33
Editor(s): Valero, M.; Joe, K.; Kitsuregawa, M.; Tanaka, H.
Publisher: Springer-Verlag, Berlin, Germany
Publication Date: 2000 Country of Publication: Germany xv+595 pp.
ISBN: 3 540 41128 3 Material Identity Number: XX-2001-00205
Conference Title: High Performance Computing. Third International Symposium, ISHPC 2000
Conference Date: 16-18 Oct. 2000 Conference Location: Tokyo, Japan
Language: English Document Type: Conference Paper (PA)
Treatment: Practical (P)
Abstract: The M-Machine's combined hardware-software shared- **memory** system provides significantly lower remote **memory** latencies than software DSM systems while retaining the flexibility of software DSM. This system is based around four hardware mechanisms for shared **memory** : status bits on individual **memory** blocks, hardware translation of **memory** **addresses** to home processors, fast detection of remote accesses, and dedicated thread slots for shared- **memory** handlers. These mechanisms have been implemented on the MAP processor, and allow remote **memory** references to be completed in as little as 336 cycles at low hardware cost. (17 Refs)
Subfile: C
Descriptors: delays; shared **memory** systems; storage allocation
Identifiers: processor mechanisms; M-Machine; hardware-software shared-**memory** system; remote **memory** latencies; DSM systems; status bits; hardware translation; **memory** **addresses** ; remote access detection; dedicated thread slots; shared- **memory** handlers; MAP processor
Class Codes: C5220P (Parallel architecture)

4/5,K/2 (Item 2 from file: 2)
DIALOG(R)File 2:INSPEC

6651740 INSPEC Abstract Number: C2000-08-5440-037
Title: Smart Memories : **a modular reconfigurable architecture**
Author(s): Mai, K.; Paaske, T.; Jayasena, N.; Ho, R.; **Dally, W.J.** ; Horowitz, M.
Author Affiliation: Comput. Syst. Lab., Stanford Univ., CA, USA
Conference Title: Proceedings of 27th International Symposium on Computer Architecture (IEEE Cat. No.RS00201) p.161-71
Publisher: ACM, New York, NY, USA
Publication Date: 2000 Country of Publication: USA vi+328 pp.
ISBN: 1 58113 232 8 Material Identity Number: XX-2000-01564
U.S. Copyright Clearance Center Code: 1 58113 232 8/2000/6...$5.00
Conference Title: Proceedings of 27th International Symposium on Computer Architecture
Conference Sponsor: IEEE Comput. Soc. Tech. Committee on Comput. Archit.; ACM SIGARCH
Conference Date: 10-14 June 2000 Conference Location: Vancouver, BC, Canada
Medium: Also available on CD-ROM in PDF format
Language: English Document Type: Conference Paper (PA)
Treatment: Practical (P)
Abstract: Trends in VLSI technology scaling demand that future computing devices be narrowly focused to achieve high performance and high efficiency, yet also target the high volumes and low costs of widely applicable general purpose designs. To **address** these conflicting requirements, we propose a modular reconfigurable architecture called Smart **Memories** , targeted at computing needs in the 0.1 mu m technology generation. A Smart **Memories** chip is made up of many processing tiles, each containing local **memory** , local interconnect, and a processor core. For efficient computation under a wide class of possible applications, the **memories** , the wires, and the computational model can all be altered to match the applications. To show the applicability of this design, two very different machines at opposite ends of the architectural spectrum, the Imagine stream processor and the Hydra speculative multiprocessor, are mapped onto the Smart **Memories** computing substrate. Simulations of the mappings show that the Smart **Memories** architecture can successfully map these architectures with only modest performance degradation. (37 Refs)
Subfile: C
Descriptors: digital simulation; multiprocessing systems; performance evaluation; reconfigurable architectures
Identifiers: Smart **Memories** ; modular reconfigurable architecture; VLSI technology scaling; conflicting requirements; Imagine stream processor; Hydra speculative multiprocessor; simulations; performance degradation
Class Codes: C5440 (Multiprocessing systems); C6185 (Simulation techniques); C5470 (Performance evaluation and testing); C5220 (Computer architecture)

4/5,K/4 (Item 4 from file: 2)
DIALOG(R)File 2:INSPEC

4863546 INSPEC Abstract Number: C9503-6120-007
Title: Hardware support for fast capability-based addressing
Author(s): Carter, N.P.; Keckler, S.W.; **Dally, W.J.**
Author Affiliation: Lab. for Comput. Sci., MIT, Cambridge, MA, USA
Journal: SIGPLAN Notices vol.29, no.11 p.319-27
Publication Date: Nov. 1994 Country of Publication: USA
CODEN: SINODQ ISSN: 0362-1340
Conference Title: Sixth International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS-VI)
Conference Sponsor: ACM; IEEE Comput. Soc
Conference Date: 4-7 Oct. 1994 Conference Location: San Jose, CA, USA
Language: English Document Type: Conference Paper (PA); Journal Paper (JP)
Treatment: Practical (P)
Abstract: Traditional methods of providing protection in **memory** systems do so at the cost of increased context switch time and/or increased storage to record access permissions for processes. With the advent of computers that support cycle-by-cycle multithreading, protection schemes that increase the time to perform a content switch are unacceptable, but protecting unrelated processes from each other is still necessary if such machines are to be used in non-trusting environments. The paper examines guarded pointers, a hardware technique which uses tagged 64-bit pointer objects to implement capability based **addressing** . Guarded pointers encode a segment descriptor into the upper bits of every pointer, eliminating the indirection and related performance penalties associated with traditional implementations of capabilities. All processes share a single 54-bit virtual **address** space, and access is limited to the data that can be referenced through the pointers that a process has been issued. Only one level of **address** translation is required to perform a **memory** reference. Sharing data between processes is efficient, and protection states are defined to allow fast protected subsystem calls and create unforgeable data keys. (25 Refs)
Subfile: C

4/5,K/5 (Item 5 from file: 2)
DIALOG(R)File 2:INSPEC

04328677 INSPEC Abstract Number: C9303-5440-001
Title: The J-machine: a fine-grain parallel computer
Author(s): **Dally, W.J.** ; Chien, A.; Davison, R.; Fiske, J.A.S.; Furman, S.; Fyler, G.; Gaunce, D.B.; Horwat, W.; Kaneshiro, S.; Keen, J.S.; Lethin, R.A.; Noakes, M.; Nuth, P.R.; Spertus, E.; Totty, B.; Wallach, D.; Wills, D.S.
Author Affiliation: Artificial Intelligence Lab., MIT, Cambridge, MA, USA
Journal: Computing Systems in Engineering vol.3, no.1-4 p.7-15
Publication Date: 1992 Country of Publication: UK
CODEN: COSEEO ISSN: 0956-0521
U.S. Copyright Clearance Center Code: 0956-0521/92/$5.00+.00
Conference Title: Symposium on High-Performance Computing for Flight Vehicles
Conference Sponsor: Univ. Virginia; George Washington Univ.; NASA
Conference Date: 7-9 Dec. 1992 Conference Location: Washington, DC, USA
Language: English Document Type: Conference Paper (PA); Journal Paper (JP)
Treatment: Practical (P)
Abstract: The MIT J-machine is a fine-grain concurrent computer that provides low-overhead mechanisms for parallel computing. Prototype J-machines have been operational since July 1991. The J-machine communication mechanism permits a node to send a message to any other node in the machine in <2 mu s. On message arrival, a task is created and dispatched in <1 mu s. A translation mechanism supports a global virtual **address** space. These mechanisms efficiently support most proposed models of concurrent computation and allow parallelism to be exploited at a grain size of 10 operations. The hardware is an ensemble of up to 65536 nodes each containing a 36-bit processor, 4 K 36-bit words of on-chip **memory** , 256 K words of DRAM and a router. The nodes are connected by a high-speed three-dimensional mesh network. (24 Refs)
Subfile: C

4/5,K/6 (Item 6 from file: 2)
DIALOG(R)File 2:INSPEC

04139054 INSPEC Abstract Number: C9206-6120-003
Title: A fast translation method for paging on top of segmentation
Author(s): **Dally, W.J.**
Author Affiliation: Artificial Intelligence Lab., MIT, Cambridge, MA, USA
Journal: IEEE Transactions on Computers vol.41, no.2 p.247-50
Publication Date: Feb. 1992 Country of Publication: USA
CODEN: ITCOB4 ISSN: 0018-9340
U.S. Copyright Clearance Center Code: 0018-9340/92/$03.00
Language: English Document Type: Journal Paper (JP)
Treatment: Practical (P)
Abstract: A description is presented of a fast, one-step translation method that implements paging on top of segmentation. This method translates a virtual **address** into a physical **address** , performing both the segmentation and paging translations, with a single TLB (translation lookaside **buffer**) read and a short add. Previous methods performed this translation in two steps and required two TLB reads and a long add. Using the fast method, the fine-grain protection and relocation of segmentation combined with paging can be provided with delay and complexity comparable to paging-only systems. This method allows small segments, particularly important in object-oriented programming systems, to be managed efficiently. (15 Refs)
Subfile: C
Descriptors: virtual storage
Identifiers: fine grain relocation; paging; segmentation; one-step translation; virtual **address** ; physical **address** ; translation lookaside **buffer** ; TLB reads; fine-grain protection; object-oriented programming
Class Codes: C6120 (File organisation)

Author(s): **Dally, W.J.**
...Abstract: step translation method that implements paging on top of segmentation. This method translates a virtual **address** into a physical **address** , performing both the segmentation and paging translations, with a single TLB (translation lookaside **buffer**) read and a short add. Previous methods performed this translation in two steps and required...
...Identifiers: virtual **address** ; ...

...physical **address** ; ...

...translation lookaside **buffer** ;

4/5,K/12 (Item 2 from file: 6)
DIALOG(R)File 6:NTIS

1430460 NTIS Accession Number: AD-A204 210/9
J-Machine: System Support for Actors
(**Memorandum** rept)
Dally, W. J.
Massachusetts Inst. of Tech., Cambridge. Microsystems Research Center.
Corp. Source Codes: 001450004; 417195
Report No.: VLSI-M-88-491
Dec 88 33p
Languages: English Document Type: Translation
Journal Announcement: GRAI8912
Order this product from NTIS by: phone at 1-800-553-NTIS (U.S. customers); (703)605-6000 (other countries); fax at (703)321-8547; and email at orders@ntis.fedworld.gov. NTIS is located at 5285 Port Royal Road, Springfield, VA, 22161, USA.
NTIS Prices: PC A03/MF A01
Country of Publication: United States
Contract No.: N00014-87-K-0825; N00014-85-K-0124
The J-Machine in concert with its operating system kernel, JOSS, provides low-overhead system services to support actor programming systems. The J-Machine is not specialized to actor systems: instead, it provides primitive mechanisms for communication, synchronization, and translation. Communication mechanisms are provided that permit a node to send a message to any other node in the machine in < 2 microsecs. On message arrival, a task is created and dispatched in < 1 microsecs. A translation mechanism supports a global virtual **address** space. These mechanisms efficiently support most proposed models of concurrent computation. The hardware is an ensemble of up to 65,536 nodes each containing a 36-bit processor, 4K 36-bit words of **memory** , and a router. The nodes are connected by a highspeed 3-D mesh network. The design was chosen to make the most efficient use of available chip and board area. Keywords: Parallel processors. (KR)
Descriptors: *Message processing; *Parallel processors; Arrival; Communication and radio systems; Computations; Computer programming; Efficiency; Models; Supports
Identifiers: *Computer architecture; Translations; NTISDODXA
Section Headings: 62A (Computers, Control, and Information Theory--Computer Hardware); 62B (Computers, Control, and Information Theory--Computer Software)

(**Memorandum** rept)
Dally, W. J.
... task is created and dispatched in < 1 microsecs. A translation mechanism supports a global virtual **address** space. These mechanisms efficiently support most proposed models of concurrent computation. The hardware is an...

...to 65,536 nodes each containing a 36-bit processor, 4K 36-bit words of **memory** , and a router. The nodes are connected by a highspeed 3-D mesh network. The...

4/5,K/13 (Item 3 from file: 6)
DIALOG(R)File 6:NTIS

1413069 NTIS Accession Number: AD-A200 789/6
Fine-Grain Message-Passing Concurrent Computers
(**Memorandum** rept)
Dally, W. J.
Massachusetts Inst. of Tech., Cambridge. Microsystems Research Center.
Corp. Source Codes: 001450004; 417195
Report No.: VLSI-MEMO-88-454
Aug 88 13p
Languages: English
Journal Announcement: GRAI8907
Order this product from NTIS by: phone at 1-800-553-NTIS (U.S. customers); (703)605-6000 (other countries); fax at (703)321-8547; and email at orders@ntis.fedworld.gov. NTIS is located at 5285 Port Royal Road, Springfield, VA, 22161, USA.
NTIS Prices: PC A03/MF A01
Country of Publication: United States
Fine-grain concurrent computers, by operating at a fine grain, increase the amount of concurrency that can be efficiently exploited in a given problem. Programming is simplified because programs may be partitioned into natural units of methods and objects and these objects are **addressed** uniformly whether they are local or remote. The construction of these machines poses challenging problems in reducing overhead, increasing communication bandwidth, and developing resource management techniques. This paper describes this class of machines, the challenges posed by their construction, and recent progress toward meeting these challenges. Keywords; computers; manufacturing; fine grain concurrent computers, (kr)
Descriptors: *Computers; Bandwidth; Communication and radio systems; Machines; Resource management
Identifiers: *Fine grain concurrent computers; NTISDODXA
Section Headings: 62A (Computers, Control, and Information Theory--Computer Hardware)

(**Memorandum** rept)
Dally, W. J.
... programs may be partitioned into natural units of methods and objects and these objects are **addressed** uniformly whether they are local or remote. The construction of these machines poses challenging problems...

4/5,K/14 (Item 4 from file: 6)
DIALOG(R)File 6:NTIS

1383750 NTIS Accession Number: AD-A194 566/6
Concurrent Computer Architecture
Dally, W. J.
Massachusetts Inst. of Tech., Cambridge. Artificial Intelligence Lab.
Corp. Source Codes: 001450241; 407483
Report No.: VLSI-MEMO-87-422
Nov 87 30p
Languages: English
Journal Announcement: GRAI8820
Order this product from NTIS by: phone at 1-800-553-NTIS (U.S. customers); (703)605-6000 (other countries); fax at (703)321-8547; and email at orders@ntis.fedworld.gov. NTIS is located at 5285 Port Royal Road, Springfield, VA, 22161, USA.
NTIS Prices: PC A03/MF A01
Country of Publication: United States
Contract No.: N00014-80-C-0622; N00014-85-K-0124
Present generation concurrent computers offer performance greater than vector supercomputers and are easily programmed by non-experts. Evolution of VLSI technology and a better understanding of concurrent machine organization have led to substantial improvements in the performance of numerical processors, symbolic processors, and communication networks. A 100MFLOPS arithmetic chip and a 5 us latency communication network are under construction. Low-latency communication and task switching simplify concurrent programming by removing considerations of grain size and locality. A message-passing concurrent computer with a global virtual **address** space provides programmers with both a shared **memory** , and message-based communication and synchronization. This paper describes recent advances in concurrent computer architecture drawing on examples from the J-Machine, and experimental concurrent computer under development at MIT.
Descriptors: Communications networks; *Computer architecture; *Switching; Grain size; **Memory** devices; Programmers; Supercomputers; Time sharing; Vector analysis
Identifiers: NTISDODXA

4/5,K/15 (Item 1 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

03480140 E.I. Monthly No: EI9209110567
Title: The message-driven processor: A multicomputer processing node with efficient mechanisms.
Author: **Dally, William J.** ; Fiske, J. A. Stuart; Keen, John S.; Lethin, Richard A.; Noakes, Michael D.; Nuth, Peter R.; Davison, Roy E.; Fyler, Gregory A.
Source: IEEE Micro v 12 n 2 Apr 1992 p 23-39
Publication Year: 1992
CODEN: IEMIDZ ISSN: 0272-1732
Language: English
Document Type: JA; (Journal Article) Treatment: A; (Applications); X; (Experimental)
Journal Announcement: 9209
Abstract: The message-driven processor (MDP), a 36-b, 1.1-million transistor, VLSI microcomputer specialized to operate efficiently in a multicomputer, is described. The MDP chip includes a processor, a 4,096-word by 36-b **memory** , and a network port. An on-chip **memory** controller with error checking and correction (ECC) permits local **memory** to be expanded to one million words by adding external DRAM chips. The MDP incorporates primitive mechanisms for communication, synchronization, and naming which support most proposed parallel programming models. The MDP system architecture, instruction set architecture, network architecture, implementation, and software are discussed. 26 Refs.
Descriptors: *COMPUTER SYSTEMS, DIGITAL--*Multiprocessing; COMPUTER SYSTEMS, DIGITAL--Parallel Processing; COMPUTERS, MICROCOMPUTER; INTEGRATED CIRCUITS, VLSI
Identifiers: MESSAGE-DRIVEN PROCESSOR; TASK SCHEDULING; **ADDRESS** ARITHMETIC UNIT; J-MACHINE; CONCURRENT SMALLTALK
Classification Codes:
722 (Computer Hardware); 723 (Computer Software)
72 (COMPUTERS & DATA PROCESSING)

```
Set     Items   Description
S1      266759  BUFFER? OR CACHE? OR TEMPORAR?()(STORAGE? OR MEMOR?)
S2      492701  ADDRESS? OR LOCATION?
S3     1654752  CHANG? OR REARRANG? OR SORT OR RESORT OR REORDER? OR MODIF?
S4        2123  (NEW OR DIFFERENT)()(ORDER? OR ARRANGE?)
S5     2544895  ARRAY? OR CELL? OR STORAGE? OR MEMOR? OR RAM OR PROM OR EP-
              ROM OR EEPROM OR ROM
S6       16985  LIFO OR FIFO OR (LAST OR FIRST)()("IN" OR OUT)
S7         129  S1 AND S2 AND S3(2N)(ORDER? OR SEQUENC?)
S8          14  S1 AND S2 AND S4
S9         143  S7 OR S8
S10         36  S9 AND IC=(G06F-012? OR G06F-013?)
S11        381  S3 AND S6 AND S1
S12        110  S2 AND S11
S13         40  S12 AND IC=(G06F-012? OR G06F-013?)
S14         76  S10 OR S13
S15         56  S14 NOT AD=19980914:20010914
S16         55  S15 NOT AD=20010914:20040609
S17      14027  S2(5N)(S3 OR S4 OR S6)
S18         26  S16 AND S17
S19         26  IDPAT (sorted in duplicate/non-duplicate order)
S20         24  IDPAT (primary/non-duplicate records only)
File 347:JAPIO Nov 1976-2004/Jan(Updated 040506)
         (c) 2004 JPO & JAPIO
File 350:Derwent WPIX 1963-2004/UD,UM &UP=200435
         (c) 2004  Thomson Derwent
```

20/5/1 **(Item 1 from file: 350)**
DIALOG(R)File 350:Derwent WPIX

012913843 **Image available**
WPI Acc No: 2000-085679/200007
XRPX Acc No: N00-067173
Page storing FIFO 's used in graphics memory controller
Patent Assignee: HEWLETT-PACKARD CO (HEWP)
Inventor: SCHINNERER J A
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 6002412	A	19991214	US 97866820	A	19970530	200007	B

Priority Applications (No Type Date): US 97866820 A 19970530
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6002412	A		18	G06F-013/16	

Abstract (Basic): US 6002412 A
NOVELTY - An input bus receives sequence of data references each having an **address** with a page. The received sequence has data references with same page arranged non-sequentially. A **reordering** is performed which arranges data references with same page to be arranged sequentially and output via output bus.
DETAILED DESCRIPTION - An INDEPENDENT CLAIM is also included for a method for optimizing frame **buffer** memory performance.
USE - In graphics memory controller.
ADVANTAGE - By grouping data references having common pages together, repaging penalties at a coupled frame **buffer** memory may be reduced, thereby improving its overall performance. By **reordering** data stream references based on **addresses** of data references, it is ensured that data references referencing common **locations** are kept together, thereby enhancing memory **locations** .
DESCRIPTION OF DRAWING(S) - The figure is a block diagram of a dual pipeline memory controller system.
pp; 18 DwgNo 3/7
Title Terms: PAGE; STORAGE; **FIFO** ; GRAPHIC; MEMORY; CONTROL
Derwent Class: T01
International Patent Class (Main): **G06F-013/16**
File Segment: EPI

20/5/7 **(Item 7 from file: 350)**
DIALOG(R)File 350:Derwent WPIX

009729656 **Image available**
WPI Acc No: 1994-009506/199402
XRPX Acc No: N94-007656

Timing control for digital audio buffer in video interface - inputs data to buffer between video sync. signals and empties data at lower rate, with read and write pointers subject to holding to balance audio timing

Patent Assignee: AMPEX SYSTEMS CORP (AMPE)
Inventor: KLINGLER K L; KLINGER K L
Number of Countries: 011 Number of Patents: 004
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 577216	A1	19940105	EP 93201895	A	19930629	199402	B
CA 2099689	A	19940102	CA 2099689	A	19930629	199412	
JP 6096574	A	19940408	JP 93162766	A	19930630	199419	
US 5323272	A	19940621	US 92907426	A	19920701	199424	

Priority Applications (No Type Date): US 92907426 A 19920701
Cited Patents: 2.Jnl.Ref; EP 178075; EP 312239; EP 395210; JP 2283149; JP 57066551
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 577216	A1	E	8	H04N-005/92	
Designated States (Regional): AT CH DE FR GB IT LI NL					
JP 6096574	A		8	G11C-007/00	
US 5323272	A		8	G11B-005/00	
CA 2099689	A			H04N-005/78	

Abstract (Basic): EP 577216 A

The digital video and audio interfacing system includes a **FIFO buffer** . This receives audio data interspersed in the video data and outputs the data at a lower rate. The **FIFO** 's (100) fullness is monitored and maintained in response to an external signal. When this signal occurs the **FIFO** read and/or write **addresses** are **modified** to balance the **FIFO** contents.

When the **FIFO** is over an upper storage threshold or an upper time delay limit, the write pointer is held to cause overwriting of the last data. Similarly, on **buffer** low threshold or low time delay the read pointer is held to cause re-reading.

ADVANTAGE - Provides simple balancing **buffer** and avoids 'clips' and 'pops'. Eliminates unpleasant sound effects when multiple data samples are skipped or repeated in series. MAintains synchronisation between audio and video data.

Dwg.1/3

Title Terms: TIME; CONTROL; DIGITAL; AUDIO; **BUFFER** ; VIDEO; INTERFACE; INPUT; DATA; **BUFFER** ; VIDEO; SYNCHRONOUS; SIGNAL; EMPTY; DATA; LOWER; RATE; READ; WRITING; POINT; SUBJECT; HOLD; BALANCE; AUDIO; TIME
Index Terms/Additional Words: **FIFO_F IRST-I N-FI** ; **FIRST - IN - FIRST - OUT**
Derwent Class: T01; W04
International Patent Class (Main): G11C-007/00; H04N-005/78; H04N-005/92
International Patent Class (Additional): G06F-005/06; **G06F-012/08** ; G11B-005/02; G11B-020/10; H04N-005/907; H04N-005/93
File Segment: EPI

20/5/8 (Item 8 from file: 350)
DIALOG(R)File 350:Derwent WPIX

009710750 **Image available**
WPI Acc No: 1993-404303/199350
XRPX Acc No: N93-312918

Stack memory system for e.g. microprocessor - includes address buffer **connected between stack pointer and** address **input section, with n bits, to generate** changed address **by inverting n-th** address **bit, in response to control signal, for output to** address **input**

Patent Assignee: MATSUSHITA ELEC IND CO LTD (MATU)
Inventor: NAKAJIMA M
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 5269012	A	19931207	US 90618861	A	19901128	199350	B

Priority Applications (No Type Date): JP 89319857 A 19891208
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 5269012	A		11	G06F-012/02	

Abstract (Basic): US 5269012 A

The stack memory includes an **address** input section, a memory element array, a stack pointer, and an **address buffer** . The **address** input section has ''n'' bits where ''n'' denotes a predetermined number. The memory element array has 2n words and is connected to the **address** input section. The stack pointer generates an **address** signal with ''n'' bits, and an n-th bit of the **address** signal is inverted by a control signal. The **address buffer** is connected between the stack pointer and the **address** input section.

The **address buffer** generates a second **address** signal from the first **address** signal, and outputs the second **address** signal to the **address** input section. The second **address** signal remains equal to the first **address** signal in bits except an n-th bit, and the n-th bit of the first **address** signal is inverted again in response to the control signal to be converted into the n-th bit of the second **address** signal.

USE/ADVANTAGE - E.g. as **last in first out LIFO** memory. High speed data saving and data return operations between stack and external memory.

Dwg.6/8

Title Terms: STACK; MEMORY; SYSTEM; MICROPROCESSOR; **ADDRESS** ; **BUFFER** ; CONNECT; STACK; POINT; **ADDRESS** ; INPUT; SECTION; N; BIT; GENERATE; **CHANGE** ; **ADDRESS** ; INVERT; N; **ADDRESS** ; BIT; RESPOND; CONTROL; SIGNAL; OUTPUT; **ADDRESS** ; INPUT
Derwent Class: T01
International Patent Class (Main): **G06F-012/02**
File Segment: EPI

20/5/10 **(Item 10 from file: 350)**
DIALOG(R)File 350:Derwent WPIX

008726662 **Image available**
WPI Acc No: 1991-230677/199132
Dual-port store for real-time signal processor - exchange between I-O buffer and storage area is completed using one counter changing **reference** address order **NoAbstract**
Patent Assignee: JIANG NANFENG (JIAN-I)
Inventor: JIANG N; LIU Y; XIAO Y
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
CN 1047406	A	19901128	CN 89102868	A	19890508	199132	B

Priority Applications (No Type Date): CN 89102868 A 19890508
Title Terms: DUAL; PORT; STORAGE; REAL-TIME; SIGNAL; PROCESSOR; EXCHANGE; I-O; **BUFFER** ; STORAGE; AREA; COMPLETE; ONE; COUNTER; CHANGE; REFERENCE; **ADDRESS** ; ORDER; NOABSTRACT
Derwent Class: T01
International Patent Class (Additional): **G06F-012/00**
File Segment: EPI

20/5/13 **(Item 13 from file: 350)**
DIALOG(R)File 350:Derwent WPIX

008395361 **Image available**
WPI Acc No: 1990-282362/199037
XRPX Acc No: N90-217832
Cache **memory** address modifier **- dynamically alters catch block fetch sequence using polling circuit**
Patent Assignee: GOULD INC (GOUN)
Inventor: BEARD D R; WARD W P
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 4953079	A	19900828	US 88173406	A	19880324	199037	B

Priority Applications (No Type Date): US 88173406 A 19880324

Abstract (Basic): US 4953079 A
The **cache** memory includes an **address modification** circuit for operation during a **cache** block fetch **sequence** . The **address modification** circuit is connected to a polling circuit which receives a first word **address** from other portions of the **cache** memory connected to an instruction unit. The polling circuit tests whether a memory module storing the first word is free to make a data return transfer to the **cache** memory. When the memory module indicates that it is inhibited from making the data return to the **cache** memory, the **address modification** circuit selects in order of priority the next word in a **cache** block to be fetched and polls a memory module storing the next word.
Word **address** selection and polling continues until a free memory module responds or until all words in the **cache** block have been fetched from main memory.
ADVANTAGE - Enhances efficiency of **cache** block fetch square.
(17pp dwg.No.4/7)
Title Terms: **CACHE** ; MEMORY; **ADDRESS** ; MODIFIED; DYNAMIC; ALTER; CATCH; BLOCK; FETCH; SEQUENCE; POLL; CIRCUIT
Derwent Class: T01
International Patent Class (Additional): **G06F-012/06** ; **G06F-013/00**
File Segment: EPI

20/5/18 **(Item 18 from file: 350)**
DIALOG(R)File 350:Derwent WPIX

001474614
WPI Acc No: 1976-D7521X/197616
Memory access technique for high speed buffer **system - has read only memory connected to temporary** address **store associative memory**
Patent Assignee: DATA GENERAL CORP (DATG)
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
US 3949369	A	19760406				197616 B

Priority Applications (No Type Date): US 74436023 A 19740123

Abstract (Basic): US 3949369 A
The digital computer system has a main memory operable at a first speed, a high speed **buffer** operating at a second speed for temporarily storing selected portions of the main memory and an associative memory for temporarily storing selected main memory **addresses** and comparing the stored **addresses** with a newly received **address** in a read/write operation to generate comparison data. A read only memory having a bit configuration reflecting an algorithm, connected to the associative memory generates a **new order** of priority for the memory **address** stored in the associative memory. A storage unit connected from the read only memory stores that order of priority for subsequent feedback.
Title Terms: MEMORY; ACCESS; TECHNIQUE; HIGH; SPEED; **BUFFER** ; SYSTEM; READ ; MEMORY; CONNECT; TEMPORARY; **ADDRESS** ; STORAGE; ASSOCIATE; MEMORY
Derwent Class: T01
International Patent Class (Additional): **G06F-013/00**
File Segment: EPI

04646288 **Image available**

METHOD AND DEVICE FOR TRANSFERRING DATA RELATING TO MULTI-CPU

PUB. NO.: 06-318188 [JP 6318188 A]
PUBLISHED: November 15, 1994 (19941115)
INVENTOR(s): TACHIBANA TAKETO
ARAI TAKAO
APPLICANT(s): NIPPON AVIONICS CO LTD [327329] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 05-106699 [JP 93106699]
FILED: May 07, 1993 (19930507)
INTL CLASS: [5] G06F-015/16; **G06F-013/14**
JAPIO CLASS: 45.4 (INFORMATION PROCESSING -- Computer Applications); 45.1 (INFORMATION PROCESSING -- Arithmetic Sequence Units); 45.2 (INFORMATION PROCESSING -- Memory Units)

ABSTRACT

PURPOSE: To make it possible to transfer any of individual massive data and the same massive data at high speed by **changing** the port **addresses** of plural **FIFO buffer** data writing ports.

CONSTITUTION: A controlling CPU 11 allocates data writing port **addresses** for **FIFO buffers** 13 to the same **address** through a port **address** control part 15 in data transfer control circuit 12 at first. The CPU 11 writes data in the **address** to write the same data in all the **buffers** 13. Then the data are transferred to respective sub-CPUs 14. After completing the transfer of the same data, the CPU 11 individually allocates writing port **addresses** to the **buffers** 13 through the control part 15 in order to transfer individual data. Then the CPU 11 successively writes data to be transferred to the **buffers** 13, and after completing data writing, the written data are transferred to the corresponding sub-CPUs 14.

03770158 **Image available**

ADDRESS CONVERSION **BUFFER** CONTROLLER

PUB. NO.: 04-135258 [JP 4135258 A]
PUBLISHED: May 08, 1992 (19920508)
INVENTOR(s): MOCHIZUKI HISAO
APPLICANT(s): KOUFU NIHON DENKI KK [000000] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 02-258734 [JP 90258734]
FILED: September 27, 1990 (19900927)
INTL CLASS: [5] **G06F-012/10**
JAPIO CLASS: 45.2 (INFORMATION PROCESSING -- Memory Units)
JOURNAL: Section: P, Section No. 1410, Vol. 16, No. 404, Pg. 145, August 26, 1992 (19920826)

ABSTRACT

PURPOSE: To shorten time for TLB access for obtaining a real **address** from a logical **address** by exchanging the objective logical **address** of an index with a specified **address** conversion **buffer** TLB when the **address** is a branching instruction and looped, and applying the priority right of the index to the TLB.

CONSTITUTION: When it is judged by setting a branching instruction flag from a request source to a branching instruction flag register 11 that the logical **address** is the fetch request of the branching instruction and looped, only one pair of **address** conversion indexed from TLB 30-33 group applied to priority order of the index between loops are exchanged between the TLB 30 and the TLB 33, for example, having the lowest priority order of the index. The pair of **address** conversion between loops are stored in one TLB 33 and in the next loop, the pair of **address** conversion is preferentially indexed from the TLB 33 storing the pair of **address** conversion between loops while **changing** the priority **order** of the index. Thus, the time for TLB access for obtaining the real **address** from the logical **address** can be shortened.

02275058 **Image available**
CONTROLLER FOR DIRECT MEMORY ACCESS

PUB. NO.: 62-191958 [JP 62191958 A]
PUBLISHED: August 22, 1987 (19870822)
INVENTOR(s): TONO KAORU
APPLICANT(s): NEC CORP [000423] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 61-034372 [JP 8634372]
FILED: February 18, 1986 (19860218)
INTL CLASS: [4] **G06F-013/28**
JAPIO CLASS: 45.2 (INFORMATION PROCESSING -- Memory Units)
JOURNAL: Section: P, Section No. 664, Vol. 12, No. 43, Pg. 147, February 09, 1988 (19880209)

ABSTRACT

PURPOSE: To execute continuously a direct memory access to an **address** space accompanying the **change** of higher **order address** information by comparing the successively stepping **address** information sent to an external memory device with the prescribed **address** information set beforehand and sending coincident information to the external part.

CONSTITUTION: A DMA controller 1 has an **address** counter 2 to store the lower order 16 bits of a transferring starting **address** and step, thereafter, only at the number of times of transfer, an adding part to step an **address** counter 2 besides a register to store the number of times of the transfer, and a higher order 8 bit (b) of the **address** counter 2 is transferred to a **buffer** 3 and outputted as an immediate order 8 bit (d) of the **address** information to an external part. On the other hand, a lower order 8 bit (a) of the **address** counter 2 is transferred to a **buffer** 4 and outputted as the lower order 8 bit of the **address** information to the external part. Further, the DMA controller has an all 1 detecting circuit 5 as a comparing means, and the detecting circuit 5, when the higher order 8 bit (b) and the lower order 8 bit (a) come to be all 1, outputs a carry (e) to the external part.

20/5/24 **(Item 24 from file: 347)**
DIALOG(R)File 347:JAPIO

00783429 **Image available**
INTERFACE CIRCUIT FOR COMMUNICATION BETWEEN PROCESSORS

PUB. NO.: 56-103729 [JP 56103729 A]
PUBLISHED: August 19, 1981 (19810819)
INVENTOR(s): FUNASHIGE HIROSHI
APPLICANT(s): NEC CORP [000423] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 55-006679 [JP 806679]
FILED: January 23, 1980 (19800123)
INTL CLASS: [3] G06F-003/00; G06F-005/06; **G06F-013/00** ; G06F-015/16; H04L-013/00
JAPIO CLASS: 45.3 (INFORMATION PROCESSING -- Input Output Units); 44.2 (COMMUNICATION -- Transmission Systems); 44.3 (COMMUNICATION -- Telegraphy); 45.2 (INFORMATION PROCESSING -- Memory Units); 45.4 (INFORMATION PROCESSING -- Computer Applications)
JOURNAL: Section: P, Section No. 88, Vol. 05, No. 175, Pg. 51, November 11, 1981 (19811111)

ABSTRACT

PURPOSE: To reduce the delay in data transfer, by making the giving and reception of communication data between processors with **first - in** /first-on **buffer** memory, making automatical the reception/giving sequence of communication data, and making unnecessary the sequence program.

CONSTITUTION: **First - in / first - out buffer** memories FIFO0,1 are connected between input-output buses 0 and 1 connected between a plurality of processors 0,1, allowing to receive and give the communication data between CPUs 0,1 and the same. **Address** conversion circuits ATL0,1, selection circuit SEL0,1, and main memories MM0,1 are connected to this CPU1, and circuits ATL0,1 are respectively connected to FIFOs 0,1. Further, FIFOs 0,1 output a signal indicating the presence of data to be read in, the reception/giving sequence of communication data is automatically started, and a signal indicating the overflow of write-in data is output when overflow, circuits ATL0,1 **change** the **address** to other **address** and the delay in the data is decreased.

```
Set     Items   Description
S1     217204   BUFFER? OR CACHE? OR TEMPORAR?()(STORAGE? OR MEMOR?)
S2    3499021   ADDRESS? OR LOCATION?
S3    6318002   CHANG? OR REARRANG? OR SORT OR RESORT OR REORDER? OR MODIF?
S4     171587   (NEW OR DIFFERENT)()(ORDER? OR ARRANGE?)
S5    3265078   ARRAY? OR CELL? OR STORAGE? OR MEMOR? OR RAM OR PROM OR EP-
            ROM OR EEPROM OR ROM
S6      20519   FIFO OR LIFO
S7      13899   FIRST()OUT
S8      30331   (S6 OR S7)
S9         20   S1(10N)S2(2N)S3(2N)(ORDER? OR SEQUENCE?)
S10         1   S1(10N)S2(10N)S4
S11        36   S8(S)(S2(2N)S3 OR S4)
S12         2   S1(S)S2(S)S4
S13        58   S9 OR S10 OR S11 OR S12
S14        49   RD (unique items)
S15        40   S14 NOT PY>1998
S16        38   S15 NOT PD=19980914:20010914
S17        38   S16 NOT PD=20010914:20040609
File 160:Gale Group PROMT(R) 1972-1989
         (c) 1999 The Gale Group
File 635:Business Dateline(R) 1985-2004/Jun 05
         (c) 2004 ProQuest Info&Learning
File  15:ABI/Inform(R) 1971-2004/Jun 07
         (c) 2004 ProQuest Info&Learning
File  16:Gale Group PROMT(R) 1990-2004/Jun 08
         (c) 2004 The Gale Group
File   9:Business & Industry(R) Jul/1994-2004/Jun 07
         (c) 2004  The Gale Group
File 810:Business Wire 1986-1999/Feb 28
         (c) 1999 Business Wire
File 647:CMP  Computer Fulltext 1988-2004/May W5
         (c) 2004 CMP Media, LLC
File 148:Gale Group Trade & Industry DB 1976-2004/Jun 08
         (c)2004 The Gale Group
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17/3,K/13 (Item 3 from file: 16)
DIALOG(R)File 16:Gale Group PROMT(R)

03783154 Supplier Number: 45383721 (USE FORMAT 7 FOR FULLTEXT)
HP Showing Architecture For 64-Bit PA-RISC MPU
Electronic News (1991), p66
March 6, 1995
Language: English Record Type: Fulltext
Document Type: Magazine/Journal; Trade
Word Count: 707

... under the umbrella term 'Intelligent Execution.'
Among Intelligent Execution features are a 56-entry instruction **reorder buffer** to support out-of- **order** execution, a branch target **address cache** , branch history table, support for multiple outstanding **cache** misses and dual integer, load/store, floating point multiply/accumulate, and divide/square root units...

17/3,K/26 (Item 4 from file: 148)
DIALOG(R)File 148:Gale Group Trade & Industry DB

08111546 SUPPLIER NUMBER: 17349913 (USE FORMAT 7 OR 9 FOR FULL TEXT)
Open-standard, synchronous protocol boosts VXIbus data-transfer rates.
Novellino, John
Electronic Design, v43, n15, p37(2)
July 24, 1995
ISSN: 0013-4872 LANGUAGE: English RECORD TYPE: Fulltext; Abstract
WORD COUNT: 926 LINE COUNT: 00074

... buffer, called a SYNC FIFO. The master initiates a synchronous transfer by setting the MXI **address - modifier** lines, placing the address on the address lines, and asserting the Address Strobe (AS) signal...